CLAIMS

1. (Currently Amended) A synchronization circuit, comprising:

a local timestamp counter configured to generate a local timestamp value; and

a processing circuit to receive externally generated synchronization pulses and to receive a predicted master timestamp value associated with a future one of the externally generated synchronization pulses, wherein the processing circuit receives the predicted master timestamp value asynchronously in Internet Protocol (IP) packets received over an IP connection,

the processing circuit to identify the local timestamp value ~~at the future received synchronization pulse~~ and synchronize the local timestamp counter with the predicted master timestamp value ~~associated with~~ upon receipt of the future one of the externally generated synchronization pulses.

2. (Previously Presented) The synchronization circuit according to claim 1 wherein the processing circuit is located in a Cable Modem Termination System (CMTS) and receives the predicted master timestamp value from another CMTS.

3. (Previously Presented) The synchronization circuit according to claim 1 wherein the Internet Protocol (IP) packets containing the master timestamp value use a multicast address.

4. (Previously Presented) The synchronization circuit according to claim 1 including a holding register configured to store the received predicted master timestamp value.

5. (Previously Presented) The synchronization circuit according to claim 2 further comprising the processing circuitry to forward the predicted master timestamp value to the another CMTS.

6. (Currently Amended) The synchronization circuit according to claim 1 wherein the synchronization pulses cycle at ~~has~~ a rate of somewhere between 8 Kilo Hertz and 1 Hertz.

7. (Previously Presented) The synchronization circuit according to claim 1 wherein the processing circuit identifies an error condition according to a number of times the local timestamp counter is synchronized with received timestamp values.

8. (Previously Presented) The synchronization circuit according to claim 1 including multiple line cards in a same Cable Modem Termination System (CMTS) chassis that each have local timestamp counters that are adjusted according to the received predicted master timestamp value and local timestamp values at the future received synchronization pulse.

9. (Original) The synchronization circuit according to claim 1 including a first CMTS including one or more line cards that are used for downstream channels and a second CMTS including one or more line cards that are used for upstream channels, cable modems receiving data on the downstream channels of the first CMTS and sending data on the upstream channels of the second CMTS.

10. (Currently Amended) A synchronization system, comprising:

a master synchronization circuit ~~configured to:~~ including

a master counter to generate respective master timestamp values varying with cycling of a clocking signal; and

a processing circuit to determine, for a given count of consecutive ones of synchronization pulses cycling less often than the clocking signal, the corresponding difference between the master timestamp values and to

~~identify a first master timestamp value associated with a first synchronization pulse and a second master timestamp value associated with a second synchronization pulse;~~

~~determine a difference between the first and second master timestamp values and an amount of time occurring between the first and second synchronization pulses;~~

~~predict the occurrence of a future synchronization pulse according to the amount of time occurring between the first and second synchronization pulses and a predetermined amount;~~

calculate a future master timestamp value by adding ~~that corresponds to the future synchronization pulse according to~~ the corresponding difference to an initial one of the master timestamp values corresponding to an initial one of the synchronizing pulses ~~between the first~~

~~and second master timestamp values and the amount of time occurring between the first and second synchronization pulses~~; and the master synchronization circuit being configured to

forward the calculated future master timestamp value to a slave synchronization circuit over a wide area network for synchronizing the value of a slave counter in the slave synchronization circuit with the future master timestamp value at a ~~the~~ future synchronization pulse generated independently of operations by the master counter and slave counter and corresponding to the given count of consecutive ones of synchronization pulses following the initial one of the synchronization pulses.

11. (Previously Presented) The system according to claim 10 wherein the master synchronization circuit is further configured to:

identify an actual master timestamp value corresponding to the future synchronization pulse when the future synchronization pulse occurs;

determine whether a difference between the actual master timestamp value and the future master timestamp value is within a predetermined range; and

send an error message to a slave synchronization circuit when the difference between the actual master timestamp value and the future master timestamp value is not within a predetermined range that causes the slave synchronization circuit to take over operations as the master synchronization circuit.

12. (Previously Presented) The system according to claim 11 wherein the slave synchronization circuit is configured to calculate and forward new future master timestamp values in response to receiving the error message.

13. (Previously Presented) The system according to claim 12 including a first Cable Modem Termination Systems (CMTS) having a first chassis containing the master synchronization circuit and a second CMTS having a second separate chassis containing the slave synchronization circuit.

14. (Previously Presented) The system according to claim 13 including multiple lines cards in at least one of the first and second CMTS that includes multiple slave circuits each

synchronized with the future master timestamp value at the future synchronization pulse when the difference between the actual master timestamp value and the future master timestamp value is within the predetermined range.

15. (Previously Presented) The system according to claim 10 wherein the slave synchronization circuit adjusts the received calculated future master timestamp value according to an amount of delay associated with receiving the synchronization pulses.

16. (Previously Presented) A method for synchronizing circuitry, comprising:
receiving an extrapolated master timestamp value for an upcoming time reference in an Internet Protocol (IP) packet over an asynchronous Internet connection;
generating a local timestamp value;
comparing the local timestamp value at the upcoming time reference with the extrapolated master timestamp value; and
synchronizing the local timestamp value with the extrapolated master timestamp value according to the comparison.

17. (Previously Presented) A method according to claim 16 including:
identifying a period between synchronization pulses;
extrapolating a time for a future synchronization pulse by adding one of the synchronization pulses to the period multiplied by a predetermined amount; and
extrapolating the master timestamp value by adding a master timestamp value for the one of the synchronization pulses and the predetermined amount multiplied by a difference between two previous master timestamp values.

18. (Previously Presented) A method according to claim 16 including receiving the extrapolated master timestamp value from a first cable modem termination system (CMTS) and using the extrapolated master timestamp value to synchronize a timing circuit in a second CMTS.

19. (Original) A method according to claim 16 including:

synchronizing the timing circuitry in a first Cable Modem Termination System (CMTS) with the timing circuitry in a second CMTS;

using the first CMTS to send data to cable modems; and

using the second CMTS to receive data from the same cable modems.

20. (Previously Presented) A method according to claim 16 further including:

receiving an error message indicating that the predicted master timestamp value is not equal to an actual master timestamp value for a next synchronization pulse;

predicting a new master timestamp value in response to the error message; and

sending the predicted new master timestamp value to a generation source of a message including the received extrapolated master timestamp value.

21. (Previously Presented) The synchronization circuit of claim 1 wherein the predicted master timestamp value is equal to a sum of an actual master timestamp value for a previous synchronization pulse and a predetermined amount multiplied by a difference between two previous actual master timestamp values.

22. (Previously Presented) The synchronization circuit of claim 21 wherein the predetermined amount is equal to a quotient of a difference in time between the previous synchronization pulse and a next synchronization pulse divided by a period between synchronization pulses that corresponds to the two previous actual master timestamp values.